DECEMBER 2004

TDK 71M651x Power Meter IC Frequently Asked Questions

12/20/2004 3:30 PM

meter.support@tsc.tdk.com

This product is sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement and limitation of liability. TDK Semiconductor Corporation (TSC) reserves the right to make changes in specifications at any time without notice. Accordingly, the reader is cautioned to verify that the data sheet is current before placing orders. TSC assumes no liability for applications assistance.

TDK Semiconductor Corp., 6440 Oak Canyon Rd., Irvine, CA 92618
TEL (714) 508-8800, FAX (714) 508-8877, http://www.tdksemiconductor.com

© 2004 TDK Semiconductor Corporation

Contents

Contents 2
Metering Methods and Connections 3
Pulse Frequency and Width 7
Metering Accuracy and Harmonics 8
Sensors and Analog Front End 8
Multiplexer and ADC 10
Memory and Memory Security 12
Power Fail Circuitry, Reset and Watchdog 13
Temperature Compensation 15
Calibration 17
CE Features 18
RTC, Clock and Timers 19
Digital I/O and LCD Outputs 20
Other Interfaces (SSI, I2C, SPI, UART, RTM, Optical) 22
ICE, Programming, Debugging and Firmware 22
Tamper Detection 24
EMI/EMC 24
Voltage/Power Requirements, Battery Operation 24
Demo Board Questions 25
Scale and Other DC Applications 27
Miscellaneous 28

Metering Methods and Connections

Can the IB input in the TDK 71M6511 be used to implement a 3-wire single-phase meter or is the accuracy of this input restricted?

The IB input offers full accuracy and can be used to implement a 3-wire single-phase meter for the second current input. The multiplexer function has to be modified by selecting the proper meter equation in order to accept this input.

When connecting Neutral to V3P3A, what are the consequences concerning isolation of the IA/B/C and VA/B/C sense inputs with other parts of the 651x i.e. is there a chance that some of the inputs/outputs could be connected to Neutral due to an internal failure e.g. LCD pins or serial interface which would cause a hazard?

This is a quite common methodology with most of the metering chips for measurement.
If another signal faults by connecting to neutral, high current could result from this, but only to the extent it is provided by the power supply, which is limited to a few 50mA.
The ESD diodes in the 651x part ensure that all pins will be just a few volts from each other. Thus, if one of the pins is tied to neutral, and neutral is hot, there could be a hazard. This is not unique to the TDK 71M6511 and 71M6513. Any part that uses resistive dividers for voltage sense must have one of its pins connected to neutral.

What technique is used to introduce the 90-degree phase shift when measuring VAR in the 71M651x devices?

Our baseline CE code uses a bilinear integrator to shift voltage 90 degrees for VAR measurements. An all-pass filter along with 1/fo multiplication provides the accurate VAR measurement.

Is using V^2 and I^2 the most efficient method for calculating Apparent Power (VAh) in the TDK 71M6513 or 71M6511 devices?

Apparent power, measured in VAh, can be calculated from V^2 and I^2. However, it is more accurate for low currents, to use Wh and VARh, i.e. SQRT(Ws x Ws + VARs x VARs). This method of computation is less sensitive to broadband noise than V^2 and I^2.

How is the measurement of Vrms and Irms synchronized to the start of the period in the 71M6513 and 71M6511? Is a zero-crossing detector used?

The demo firmware accumulates V^2h and calculates average VRMS over the last 1-second interval. This is the same technique used for the power calculation. Thus, ripple rejection depends on a sufficiently long measurement interval. The compute engine has a frequency locked loop for generating a square wave of the same frequency as the fundamental input signal. This square wave signal is used by the measurement module of the compute engine for signal processing routines.

What method is used to calculate the reactive power in the TDK 71M651x devices?

In the TDK 71M651x devices, the CE demonstration code calculates reactive power by phase shifting the voltage waveform by 90 degrees. The phase shift circuit shifts all frequencies 90 degrees, but has a 1/f frequency response. The CE then precisely measures fundamental frequency and scales the phase shift circuit so it has unity gain. The result is an accurate VAR calculation for fundamental frequencies from 45 to 65 Hz. This single frequency technique is consistent with IEC62053-23 and with clause 3.1.5 in IEC62052-11 which states "Standards for reactive power apply for sinusoidal currents and voltages containing the fundamental frequency only." The advantage of this technique is that the VAR measurement will not "see" reactive power when unity power factor harmonics exist. This is not true of 'tracking delay' VAR measurements. Alternatively, VAR could be calculated from Wh and VAh, but typically the performance at low currents is inferior because of noise in the VAh calculation.

What are the V^2h, I^2h Values? How do I use them?

The accumulated volt squared and current squared values are used by the MPU to calculate RMS voltage and current from the previous measurement interval. The MPU divides by the number of samples and takes the square root. These values are also used to calculate VAh. V^2h and I^2h are also useful quantities to provide the amount of time the meter has run continuously without disruption. For example, a meter with 220V input running for 31 days a month continuously will result in a count of (31*24*220 *220).

What is the maximum phase compensation allowed in TDK 71M6511 or 71M6513 devices?

The maximum phase compensation allowed is ±7 degrees. The compensation can be provided by the INTERP constant in the CE data memory.

In the TDK 71M6511 and 71M6513, can the Wh and VARh pulses from the CE be programmed to provide +ve VARh and -ve VARh? Are the +ve and -ve signs associated with the phase angle and hence the quadrant in which the power vector is?

Yes, this is possible and is a useful quantity in four quadrant metering. The power measurement is classified as positive reactive power based on the sign of measured reactive power, which is also called lagging reactive power. Similarly, if the sign is negative the reactive power is also known as negative reactive power. These quantities are programmable by the user for pulse output.

Do the TDK 71M651x have the ability to measure DC power? Apart from the small DC input offsets, are there any other limitations?

The TDK 71M651x products do have the ability to measure DC power particularly if not measuring 3 phases of DC power.
The issue here is to separate the apparent DC power caused by the sensor and ADC offsets from the actual DC power to be measured. Some offset sources are given below:

1. ADC offset. This is probably the most significant DC error. Typical values observed in the 71M6511/13 are around 1 to 2mV. Our ADC is auto-zeroed, which means the offset is caused by layout dependent parasitic capacitance rather than MOSFET threshold mismatch. Offset in auto-zeroed systems should have a significantly tighter standard deviation and significantly lower drift over time. If the customer calibrates and subtracts the DC offset, he should be able to get a system that is probably 10x better and equivalent to around 0.1mV offset. Even better would be using one of the ADC inputs as a zero reference. Since the 6511/6513 uses no buffer amplifiers, the offset of each of the six inputs is the same. This technique would

provide an offset canceling method that would not require calibration and would be more stable over temperature and would offer much lower long-term drift. Accuracy should be quite good. The best result would come from allocating one or more of the six primary inputs as a zero reference input. The V3 input can't be used because it is referenced to VBIAS and will likely have a different offset.

2. Sensor offset. This effect could be quite significant in the case of Hall sensors or if a pre-amplifier is utilized. There is little that could be done here to fight offset.
3. Numerical calculation offset. Truncation of 2's complement words generates a negative offset. This offset can be predicted and cancelled within the CE code.

What is the common reference point for each phase for inputs to the ADC of the TDK 71M651x devices?

The common reference point is the V3P3 supply. The input stage of the ADC looks like a small capacitor that switches between the input and V3P3.

Can the EQU setting in the 71M651x devices be used to momentarily switch from 3-phase to 1-phase measurement and then back again?

Yes, one could change the equation specified by EQU on the fly. The customer would have to decide what to do with the lost 3-phase data. The demo code measures power in each phase. The three individual phase powers are manipulated according the EQU defined for operation. The demo code could be modified to permit individual phases to be output.

Can the TDK 71M651x devices measure reactive current?

Yes. Assuming that the current is 90 degrees out of phase with the voltage, the CE can certainly be programmed to measure this.
An alternative way to do this is to use the relation Reactive Current = Reactive Power/Voltage.

Can the 71M6513 device vary pulse rate between 1,600pulse/kWh and 30,000pulse/kWh? What is the maximum rate of pulse output and duty cycle of the TDK 71M6513 device?

Yes, variable pulse rate is possible. The limitation is the maximum pulse rate, rather than the number of pulses per kWh. The meter has a maximum power handling capacity of 144kW. This would correspond to 480V, 100A, 3ph, or the equivalent.
The 71M6513 limitation is that its maximum pulse rate must be less than 1/2 of the 2,520Hz ADC sample rate. Thus, a 3-phase, 480V, 200A meter must have a K >= 0.228kWs/pulse or 0.063 Wh/pulse which is equivalent to 15.8k pulses/kWh. If the meter full scale is lower, e.g. 277V, 10A, 3-phase, the value of K >= 6.5Ws/pulse or 1.83mWh/pulse which is equivalent to 546k pulses/kWh. Pulse rates faster than 1,260Hz would either require a hardware change or non-uniform spacing or would need a special CE firmware.

What is the formula (equation) of VARSUM?

VARSUM is the sum of the received and delivered reactive power in four quadrant metering, which could also be defined as the sum of lagging and leading reactive powers.

Do the 71M651x devices have the ability to measure reactive current?

Yes, reactive energy meters are described in IEC62053-23. The 71M6511 and 71M6513 devices were designed with IEC62053 in mind and exceed its accuracy requirements for both active energy and reactive energy.

Can the 71M651x devices handle both 50Hz and 60Hz line frequencies?

Yes, our demo code works properly with both 50Hz and 60Hz lines. It also works properly with frequencies above and below. This is necessary to meet the 2% frequency tolerance required in some specs.

Can the TDK 71M6513 generate 2 additional output pulse selected sources?

Yes. The 71M6513 can generate additional pulse outputs. Four outputs configured as Import W, Export W, Cap VAR, Ind VAR are quite feasible. It would be implemented with changes to both the CE and 80515 MPU code. No hardware changes need be made.

The 71M6511/3 measures both V and I and does the power calculation. But can the V and I measurements be displayed directly?

Yes. The demo code can be used to display the voltage and current.

Pulse Frequency and Width

Can the Wh and VARh pulse outputs be changed to measure other functions?

Yes.

Can the pulse widths be adjusted?

Yes. The variable PULSE_WIDTH can be used to program pulse widths other than the default 50ms.

What is the variable range of pulse rate of 71M6513 and is the step is fixed or random?

The pulse rate is programmable using the WRATE constant. The scaling is up to the programmer.

In the TDK 71M6511 and 71M6513, can the Wh and VARh pulses from the CE be programmed to provide +ve VARh and -ve VARh? Are the +ve and -ve signs associated with the phase angle and hence the quadrant in which the power vector is?

Yes, this is possible and is a useful quantity in four quadrant metering. The power measurement is classified as positive reactive power based on the sign of measured reactive power, which is also called lagging reactive power. Similarly, if the sign is negative the reactive power is also known as negative reactive power. These quantities are programmable by the user for pulse output.

Can the Wh/VARh output pulse rate of the TDK 71M6513 and 71M6511 be altered to implement an integer value?

Yes. The output pulse rate can be altered by modifying the WRATE cal constant with the on board 80515 MPU.

Metering Accuracy and Harmonics

What does the 63rd harmonic become in a 50Hz system and is it detectable?

In a 50Hz system, the 63rd harmonic is 63x50Hz = 3,150Hz. Our exact sampling frequency is 32,768Hz/13 = 2520.6Hz. The aliased signal will be 629.4Hz and will be detectable.

Sensors and Analog Front End

What is the maximum AC voltage that can be applied to the power supply on TDK 71M651x Demo Boards?

The maximum AC voltage can be applied to the demo board is 600V (RMS) with respect to Neutral. This limit is set by the 1000V rating of the C6 capacitor on the demo board. The value of the capacitor is sufficient to power the meter at 240V RMS or higher.

The voltage divider on the 71M651x demo boards seems to be much larger than would be required even to support a 480V AC phase voltage while staying within the ±250mV pk maximum voltage on the IC. Does the accuracy diminish as the maximum and minimum values are approached on the voltage and current inputs?

600V RMS is also the full-scale voltage assumed by the resistor divider. In other words, 600V (RMS) corresponds to 250mVpk at the ADC. The current scaling maps 210A (RMS) to 250mVpk. The ADC is extremely linear from 250mVpk on down. Full scale ADC clipping occurs at around 330mV, depending on the exact value of the reference. It is better to design the voltage divider to take 20% above the rated voltage to take care of thermal drifts.

Is the 71M6511/6513 able to support the use of resistive shunts to directly measure current? What is the smallest input voltage, at which 0.1% to 0.2% accuracy can be supported?

The 71M6511/613 Demo Boards were designed for use with a current transformer (CT) input and have to be modified and rerouted for a current shunt input to prevent quantization noise at the super low end shunt voltage input. Also, the CE program has to be modified to amplify the current gain 8x. With these modifications, the 71M6511/6513 has been tested with a shunt connection and its accuracy has been tested over the range of 125 to 0.1Amp. The accuracy was within 0.1% to 0.2% down to 0.3A and lower than 0.3A if the integration time was increased. This would correspond to an input amplitude of roughly 0.3mV RMS.

Does TDK recommend types of current transformers and voltage shunts and what accuracy should they have?

This is up to the meter manufacturer and desired meter specifications. The meter itself provides the signal that must be within ±250mV at the inputs of the 71M651X devices.

How can I adjust the offset between 1S and 1L? Is this done in the IC or on the board?

Offset is automatically removed within the IC as long as the analog inputs are within ±0.25V of the 3.3VDC supply to the IC. There is no additional offset adjustment required.

What are the evaluation conditions for the 71M6511 such as turns of the CT, input current at IA and calibration values?

TDK recommends using a CT with 2000:1 ratio with a 1.7Ω load resistor. This will result in 250mV at the input for 200 Amperes.

Can a Rogowski coil be directly connected to the TDK 71M6513? What does the input impedance to the ADC look like?

Yes, a Rogowski coil can be connected. When using a di/dt device such as a Rogowski coil, there may be the need to roll off high frequencies so the entire signal stays within the ±250mV range. Phase shift due to the roll-off can be compensated in the CE. The ADC input impedance is a 1pf switched capacitor at 5MHz. This gives an equivalent input impedance of 200kΩ.

I want to design a single-phase power meter with anti-tamper features that use monitoring the power of both the phase and neutral line currents. How can I implement this?

The basic requirement is to have two current inputs for monitoring both power line currents (phase and neutral). The power (KWh and KVARh) will be calculated based on the line with the higher current. When the line currents differ by more than 6.25%, the power measurement is changed to the higher current line, and vice versa. There is no problem in using both a CT and a shunt for single-phase meters.
The channel for current input with shunt has to have 8x gain in the Compute Engine program and necessary care is taken in PCB layout design to avoid crosstalk.

In general terms it can be said that the Compute Engine provides two individual registers for kWh for phase and neutral current inputs, based on the Wh register info. The MPU code can be used for verifying the tamper conditions based on the register information. Two registers for kVARh and I^2h are also provided. The new single-phase meter demo code provides the following 7 register values:

- $V_0 * I_0$ Wh register (phase current)
- $V_0 * I_0$ VARh register
- $V_0 * I_1$ Wh register (neutral current)
- $V_0 * I_1$ VARh register
- I_0^2h Phase current register
- I_1^2h Neutral current register
- V_0^2h Voltage Register.

Multiplexer and ADC

When the ADC is multiplexing between inputs, there will be a delay in time (phase error) between each sample. For instance, if V and I are sampled, they will be sampled at different times, how is the delay between the samples accounted for? Is this done automatically by the firmware?

It is important that the I and V samples of a given phase have zero relative delay. The samples are initially shifted apart in time due to the single converter. Our baseline code automatically corrects for this shift with an all-pass filter on the voltage side. This correction is robust, giving the proper correction at 50 and 60Hz, as well as higher harmonics.
The all-pass filter is controlled by a single constant. Minor adjustments to the constant permit delay compensation for phase mismatches in voltage and current sensors.

What is the sampling rate of the ADC of the 71M6511 and 71M6513, and up to what harmonic can these chips measure (measurement accuracy).

The front-end sample rate of the ADC, i.e. the speed of the modulator in the delta-sigma ADC, is 5MHz. One full cycle of 13 multiplex states occurs at 2,520Hz, i.e. each channel is sampled at 2,520Hz. The system meets all known harmonic accuracy specifications including IEC 65053-22 (5th harmonic) and the harmonic specifications published by some manufacturers that cover the range up to the 21st harmonic.

Although only one ADC is used in the 71M651x devices to reduce crosstalk between channels, how is the cross-talk between samples reduced?

The contents of the ADC decimation filter are completely cleared between samples. Also, sufficient time for the ADC modulator to settle to the new multiplexed value is provided before the filter begins calculating the new value

Does TDK have a patent on the single ADC with MUX?

TDK Semiconductor has a patent that is filed and pending.

Can I see the raw ADC samples?

The CE creates an interrupt at the 2,520Hz rate, which tells the 80515 MPU when new ADC data is available. By using RTM mode data transfer and an external processor (or a host PC running LabView software) it is possible to capture raw data. The SSI interface may also be used to get access to raw data samples.

Can you explain the input stage of the ADC i.e. how we can measure the ±250mV swing? What is the common reference point for each phase?

The common reference point is the V3P3 supply. The input looks like a small capacitor that switches between the input and V3P3.

Can the reference voltage of the ADC be made flexible in the range from 0.125V to 0.5V? Also, it should be possible to amplify its value.

First, the dynamic range of the current input is 2000:1. The current internal Vref is designed with 10ppm temperature stability.
In case the range is to be increased beyond the specification, the CE Engine input sample gain can be modified.
The 71M6511/13 have not been tested with external reference, since the internal reference is already beyond the industry standard requirement.

What is the ADC's speed when transmitting data to the MCU in the 71M6511/6513 devices?

The ADC samples 32,768/13 = 2,520 samples per second.

Is there a limitation to high frequency modulated signals that the TDK71M651x devices can detect due to the sampling rate of the ADC?

The 6513 has a sample rate of 2520 Hz. Thus the highest frequency that can be detected must be below 1260Hz.

Memory and Memory Security

Could the disabling of the emulator clock (ECK_DIS=1) in the application that is downloaded to the 71M651x devices provide some security against tampering?

When enabled, the security feature limits the ICE to global flash erase operations only. All other ICE operations are blocked. This guarantees the security of the user's MPU and CE program code. Security is enabled by MPU code that is executed in a 32 cycle pre-boot interval before the primary boot sequence begins. Once security is enabled, the only way to disable it is to perform a global erase of the flash, followed by a chip reset. Global flash erase also clears the CE program RAM.

The first 32 cycles of the MPU boot code are called the pre-boot phase because during this phase the ICE is inhibited. A read-only status bit, *PREBOOT*, identifies these cycles to the MPU. Upon completion of the pre-boot phase, the ICE can be enabled and is permitted to take control of the MPU.

SECURE, the security enable bit, is reset whenever the chip is reset. Hardware associated with the bit permits only ones to be written to it. Thus, pre-boot code may set *SECURE* to enable the security feature but may not reset it. Once *SECURE* is set, the pre-boot code is protected and no external read of program code is possible. The SECURE_E fuse must be blown to enable *SECURE* set. If SECURE_E is not blown, *SECURE* may not be set. The SECURE_E fuse may not be overridden with *FOVRIDE*.

Specifically, when *SECURE* is set:

- The ICE is limited to bulk flash erase only.
- Page zero of flash memory, the preferred location for the user's preboot code, may not be page-erased by either MPU or ICE. Page zero may only be erased with global flash erase. Note that global flash erase erases CE program RAM whether *SECURE* is set or not.
- Writes to page zero, whether by MPU or ICE are inhibited.

If the emulator clock is disabled with ECK_DIS, the emulator is indeed locked out. This would provide some measure of security, but since the bit is reset when external reset occurs, the tamperer could 'break in' to the MPU before the MPU sets the *ECK_DIS* bit. Once the meter cover has been penetrated components can be altered.

When the FLASH is programmed, is the complete FLASH erased first, ensuring that no residual program is left, before a new image is programmed?

Yes.

If customers use the unused FLASH as non-volatile storage for total energy consumption (for example), then in order to ensure that this figure is accurate, before a power failure occurs, could this mean that certain FLASH locations will be written to excessively (over the lifetime of the meter)?

Yes, the 20,000 times write limit does limit the use of flash memory for TOU data. The optimum plan would be to store as much data as fits in the battery backed XRAM and then transfer it to flash when it is full. This should minimize the amount of flash memory used. If the customer can't fit his requirements into the flash, the data can be

stored in the EEPROM, which typically has 1M write cycles. Also note that the data is written on a special event occurrence such as power failure/ or season change in TOU (time of use) metering.

Are there any methods for checking the contents of the RAM/FLASH in the TDK 71M651x devices, to ensure that no corruption has occurred during power fail, i.e. some form of checksum?

Yes, this would be a boot-up procedure implemented in 80515 MPU firmware

Why do the 71M651x devices not provide an external memory bus access to expand memory? 64K of memory is OK for a standard meter, but a pre-payment meter typically requires 128K due to the different country support, proprietary Synchronous Smart card protocols and encryption (3DES and AES)

The extra pins are expensive, both in power consumption and price. The CE is powerful enough to perform all the multiplications and accumulations with capacity left over. This is especially true in the single element residential case.

What is the main use of the RAM in the 71M6513/6511 devices?

The 71M651X have 2kB RAM for the 80515 MPU, used for metering and data storage.
1kB RAM - CE Data -- Compute Engine Data Storage.
4kB RAM - CE program -- Compute Engine program.
Is there any information on the SFRs that are implemented and how to use them other than what is in the files reg805151.h and sfrs.c?
The SFRs are described in the Software User's Manual.

How can I update flash without using the ICE?

To read values from the CE it is better to switch the CE off using the CE0 command through the serial port and then read the information. This causes the information to be consistent.

Power Fail Circuitry, Reset and Watchdog

In the TDK 71M6153 and 71M6511 devices, is the MPU involved in servicing the power fail interrupt, or is this implemented fully in hardware? What is the reaction time to a power fault?

The part has a hardware monitor to observe the power supply. Its reaction time is a few µs. The demo code does not have any fault detection in the CE, although it could certainly be added.

Do the 71M651x devices have integrated Power-On-Reset circuitry?

Yes, the 71M651x devices have on-chip power fault detection and reset circuitry. This is implemented by using the on-chip comparator for generating the Reset pulse for external devices. The trip point is programmed externally with a pair of resistors

Do the TDK 71M651x devices have the capability to reset without external stimulation?

The chip has internal detection of power_ok and power_not_ok states. It uses an external resistor divider so customers can select the trip voltage. This should be more economic than a large external RC time constant.

Are there any limitations on the reset circuit?

No, the reset circuit works well on the demo boards, properly resetting the chip on both fast and slow power up sequences.

Is the watchdog timer implemented in hardware?

Yes, the robust watchdog timer is implemented in hardware with a fixed 1.5s timeout. The generic 80515 MPU programmable watchdog timer is also present.

Do the 71M651x devices have a robust watchdog timer?

Yes. The 71M6511/6513 parts have a 1.5s independent watchdog timer that cannot be turned off by firmware. Thus, there is no WD enable flip flop that can be turned off by an ESD event. Any circuit state that causes firmware to loose control or any slow-down of the clock will be caught and will force a reboot of the chip. Although the WD timer can't be turned off by firmware, it can be disabled by connecting the V1 pin (power fault detect) to 3.3V. This is essential for initial system debug.

Do the TDK 71M651x devices power up with the watchdog timer enabled?

The chip powers up with the watchdog disabled. It will be enabled in the power-up boot sequence. Once enabled, it can't be disabled without a full chip reset.

When does the TDK 71M651x MPU exit from reset?

The MPU will exit from reset 4100 cycles of the 32kHz clock after **ResetZ** is taken High.

Does the TDK 71M651x reset input pin have a Schmitt-trigger?

No.

Is the reset timer count value (4100) programmable?

No. This time is necessary to ensure the PLL is settled and stable.

Is there is default setting of the MPU clock divider (MPU_DIV) which is always used at power-on-reset, for example 000=CKCE, or can the POR setting be defined in boot-up code?

MPU_DIV hardware default is 000. For low power, the MPU should reprogram MPU_DIV as soon as possible.

Temperature Compensation

How much can the 71M6511 compensate the thermal drift of external components?

The question is very hard to answer since the external component characteristics are unknown.
±10 PPM/°C (651XH) or ±50 PPM/°C (651X) is achieved when compensation is limited to the 71M651x device itself using the internal temperature sensor. The 651XH has a double-trimmed bad gap with predictable behavior over temperature (±10 PPM over the temperature range) that makes reading of the internal temperature sensor more accurate. The 651X has a single-trimmed band gap with ±50 PPM deviation from nominal over temperature.

In a system design, the temperature sensor inside the 71M6511 cannot always determine the temperature of the external components with 100% accuracy. Think of a meter containing the 6513H chip sensing a substrate temperature of 60°C. This could be because the external components have been heated up equally to 60°C, or because the PCB that the 6513H is mounted on is exposed to sunlight, but the other components are cold. Thus, planning of component placement, airflow and consideration of component thermal characteristics may be needed to provide accuracy.

How would a typical application in the 71M651x devices compensate for the thermal drift of external components?

The 71M651x devices can compensate for temperature variations in components by measuring its own temperature and by responding to scale factors written in its CE memory by the on-chip 80515 MPU. A typical temperature compensation program in a single-phase meter might be as follows:

1. The 80515 MPU requests the CE to measure temperature once per second. The frequency of this request is controlled completely by the 80515 MPU. In the example, we assume the 80515 MPU requests temperature each time it receives an XFER_BUSY interrupt.
2. Based on the temperature measurement, the 80515 MPU determines which parameters need to be adjusted. In this example, let's assume the 80515 MPU adjusts the gain of the voltage and current ADC outputs as well as the phase shift of the current sensor. The MPU would compensate for voltage and current gain by modifying the value of CAL_IO and CAL_V0. The amount of adjustment must be decided in advance and is read from a table whose x axis is temperature and y-axis is the amount of adjustment.

The accuracy and range limitation are shown below:
Range limitation:
The gain of the voltage and current paths are varied by multiplying by an integer gain constant. The gain will be zero when the constant is zero. Typically, the constant is 2^{14} for current and for voltage. The maximum value for either constant is 2^{15}. Thus, the adjustment range is from 0x to 2x (CE demo software limitation).
Accuracy limitation:

1. The temperature sensor measures the temperature deviation from room temperature. It is accurate to ±1 degrees at temperature extremes. It is repeatable to ±1 degree (estimated) at room temperature. Thus a probable temperature tolerance is:
   TempError(degrees) = ± (1 + (T-T_{room})0.16). This is a CE hardware limitation.
2. The typical value of the gain constant is 16384. Thus, the resolution of one step (1 LSB) is 0.0122%. This is CE demo software limitation.

3. The temperature of the 651X IC is assumed to be the same as the temperature of the component being compensated. The self-heating of the 651X IC is estimated to be less than 3 degrees.

Compensation accuracy depends on the predictability of the component being compensated.

Calibration

Do I have to follow the calibration procedure specified in the Demo Board User's Manuals?

The procedures in the Demo Board User's Manuals, based on energy collection, are a good starting point for evaluating the 6511 and 6513 chips. Users may define their own calibration procedures, which could involve measuring voltage, current and phase angle directly and then determining the calibration factors.
It is also possible to generate improved calibration procedures that take into account varying phase angles at different currents. This would require that the MPU feeds different calibration factors to the CE RAM, depending on the current that the meter encounters.

Are the Wh and VARh outputs intended to be Pulse outputs for calibration purposes?

No. The Wh and VARh results are the 71M651x device pulse generator outputs that can be used drive other pulse counters.

Is there any auto-correction in the VREF, or would this need to be implemented in the MPU by the customer using the Temp measurement?

The reference circuit (VREF) is built to be as intrinsically flat over temp as possible. Additional curvature correction is sometimes added, but this increases the variation in the temperature curve and results ultimately in worse accuracy than digital correction. This design is based on a band gap reference circuit.

What is the minimum (0000) and maximum (FFFF) input gain for V/I_CAL (in dB) in the 71M651x devices?

The voltage CAL is nominally 16384. It can vary from 0 to 32767. The result from CAL is a sample stream that has been scaled by V_CAL/16384. The dB range is therefore +6dB to -infinity. If the customer's baseline design requires a V_CAL less than 1000, the cal step size will be larger than 0.1%, which may be too coarse.
The current cal is nominally 16384 and scales the current stream by I_CAL/16384. The same digital range as for the voltage applies. Thus the dB range is +6dB to -infinity.

What value is to be used for calibration?

KVAR: Although a range for KVAR is given, the entry should stay at 1931(hex).
QUANT: These two values are the same - the UART interface treats all numbers as hex unless they are preceded with a + or - sign.

My calibration system tells me that the accuracy after calibration is changing from 0.08% to 0.25%, and then back to 0.08%. What is going on?

If the integration time over several pulses is relatively low, and if the calibration system is not synchronized to the pulses, it may sometimes catch a pulse in its time window and sometimes miss it. Make sure to use either a synchronized calibration system or a reasonably long integration time.

I calibrated the 651X chip, but now the results are worse than before. What is going on?

Make sure the calibration system applied 60° phase shift, and not –60° (300°). It is customary to use the angle by which the voltage leads the current. This means that there is a **positive** phase for **inductive** circuits since **current lags** the voltage in an inductive circuit. The phase is **negative** for a **capacitive** circuit since the **current leads** the voltage.

CE Features

Do the 71M651x devices implement something in the CE to filter out the 'ripple control' signal?

No.

In CE code at the end of each complete cycle, does the CE interrupt the MPU in order to fetch the energy values from the CE RAM? What is the cycle time, and will it vary if additional code is added? Is it possible to make the CE code interrupt the MPU at other intervals, or is the MPU responsible for accumulating the fractions of energy?

The MPU receives a CE_BUSY interrupt after each CE code pass. The other interrupt occurs once at the end of each sum interval and is called XFER_BUSY. The rate of this interrupt can be varied and is set at 1 second in the demo configuration (SUM_CYCLES and PRE_SAMPS). The energy is always accumulated by the CE, but when the CE generates XFER_BUSY, it stores the energy in registers accessible to the MPU. Upon receiving the XFER interrupt, the MPU reads the accumulated energy and updates its display, EEPROM, and whatever else is required for housekeeping. The XFER_BUSY handler of the MPU code does a number of calculations, including the calculation of RMS voltage and current and the measurement of load angles.

Is the Compute Engine (CE) code modifiable by the customer?

Yes it is. The code is stored in Flash memory.

Can CE calibration values be changed continuously without resetting the CE in the 71M651x devices?

Yes. The on-chip 80515 MPU can make "on the fly" changes to the CE data RAM. This is required for temperature correction of calibration data.

What are the limits on the Phase correction in the TDK 71M651x devices?

The demo code contains constant delay all-pass filters that adjust the voltage delay by 11/13 of one ADC sample time (7.25 degrees @ 60Hz, 6.04 degrees @ 50Hz). The all-pass delay is controlled by a parameter that can be adjusted to compensate for additional phase errors, such as caused by the CT's (5 degrees). If the delay is caused by high frequency roll-off, for instance, a better compensation method might be an additional single pole network, which would flatten the frequency response as well as the delay.

How should the I_CROSS and V_CROSS constants of the CE data memory be set in the TDK 71M6511 and 71M6513 devices?

The values of I_CROSS and V_CROSS should be set to zero.

Is the INTERP compensation already applied to the V+I samples that are stored in TDK 71M651x devices?

Yes. The compute engine aligns the current input to the voltage input based on the INTERP parameter.

RTC, Clock and Timers

Does the RTC support leap years?

Yes.

Do I have to be careful when writing data to the RTC registers? What happens if I enter a number > 31 for the day of month?

Some wrap-around will appear when the number is larger than the register should hold. However, when the register gets updated (e.g. every minute the minute register is updated), the register will go back to a “legal” number range. Generally, entries to the RTC should be checked for validity before they are written to the RTC registers.

What is the max value that can be held in the RTC before it wraps around?

The maximum RTC value is 255 years, i.e. the year 2255.

Do the 71M651x devices provide the 32K RTC clock as a buffered output?

The RTC clock is an output option of TMUXOUT.

I want to implement a 1µs timer. Having looked at the timer.c code, the T0/T1 timers have a 10ms granularity and need to be manually restarted, using the appropriate api call. I know from previous experience with 8051/52 that T0/T1 timers can be 8-bit reloadable (TxM1/M0=10 in TMOD SFR). Is this implement in the timer API? Otherwise, I will have to change the timer API, which may affect other functions within the LAPIE.

Each instruction needs 12 clock cycles so a timer with '1' works at (5/12) MHz speed meaning 2.4 microseconds. We recommend using timers for intervals of more than 100 microseconds. The current timer interval of 10ms is useful for running the APIs and to verify if there is any activity on any I/O ports.

There is a second timer (T2) mentioned in the reg80515.h file. Do I have access to T2?

No, T2 does not exist in the 71M651X and there is no MDU (Multiply Divide unit).

Is drift in the watch crystal compensated by the temperature sensor in the TDK 651x devices? What should the maximum drift of the 32K crystal (in PPM) be in order to maintain 0.1% accuracy?

Yes, it is possible to compensate for temperature drift. For this, the MPU firmware has to be modified to generate compensating coefficients by observing the real time clock on the TMUXOUT pin.
Meter accuracy is directly proportional to clock rate. Thus, 0.1% meter error occurs when the crystal is 1000PPM in error. Many production calibration procedures adjust the V and I scale to achieve correct meter reading. These procedures automatically correct for time base error.

What is the accuracy of the 32K crystal and RTC on the Demo Board over time (long term stability)? How is accuracy controlled?

The accuracy over time is guaranteed by the crystal manufacturer. Ecliptec corp (www.ecliptek.com) specifies 3ppm/year for their EC38T Series. We are careful to avoid premature aging of the crystal by minimizing its power dissipation.

Digital I/O and LCD Outputs

Can all the SEG pins and COM pins be used as DIO pins in the TDK 71M651x devices?

No. The 71M6513 has four general DIO pins (DIO0…DIO3) that are fully configurable as DIO. The four COM pins (COM0…COM3) and the 19 dedicated segment outputs (SEG0…SEG2, SEG8…SEG23) are to be used to drive LCDs only. The 18 multi-use pins SEG24/DIO4 to SEG41/DIO21 can be either LCD outputs or general DIO. The five LCD outputs SEG3…SEG7 are shared with the SSI interface and are not general DIO.

The 71M6511 has no general DIO pins. The four COM pins (COM0…COM3) and the 15 dedicated segment outputs (SEG0…SEG2, SEG8…SEG19) are to be used to drive LCDs only. The 24 multi-use pins SEG24/DIO4… SEG31/DIO11, SEG34/DIO14…SEG37/DIO17) can be either LCD outputs or general DIO. The five LCD outputs SEG3…SEG7 are shared with the SSI interface and are not general DIO.

Do the digital I/O pins in the TDK 651x devices have enough capability to drive LEDs directly?

Yes, but a current limiting resistor will be necessary to drive LED’s

Are the LCD I/Os on the TDK 71M6511/6513 capable of driving dot matrix displays (2 line x 16 characters?)?

No. The LCD can drive up to 168 individual dots (5.25 dots per character).

Can the 71M6515x devices use 3 common, 33% DC for display bright/contrast?

The 71M651X chips support this mode. There is also a voltage DAC for adjusting the contrast.

How many LCD segments can the TDK 71M651x devices drive?

The 71M6513 can use up to 42 segment pins that along the 4 COM pins can drive up to 168 LCD segments. The 71M6511 can use up to 32 segment pins that along with the 4 COM pins can drive up to 128 LCD segments. The 71M6515 does not drive an LCD.

Can programmable pulse outputs with separate pulse dividers and pulse widths implemented?

The user can use the one of general-purpose I/O ports and can program to generate desired pulse output.

How does the voltage boost work? Please explain the various pins (VDRV, VLCD) of the 6511 and 6513!

VDRV is an output that generates AC when the LCD_BSTEN bit (0x2020, bit 7) is set. If the AC from VDRV is applied via a small capacitor (e.g. 33nF) and a diode to a large reservoir capacitor (e.g. 220nF), this large capacitor builds up 5VDC. An example for this circuit is implemented in the Demo Boards. See the Demo Board User's Manuals for the schematics.
VLCD is an input. If the 651X drives 3.3V-compatible LCDs, the voltage at this input should be 3.3V. If it drives 5V LCDs, either 5VDC generated by the VDRV pin or any other 5V source should be applied to VLCD.

Other Interfaces (SSI, I2C, SPI, UART, RTM, Optical)

Does the UART speed rely on the MPU clock divider in the TDK 71M651x device?

Not until the MPU can't service the port fast enough. We are presently running 9600 baud at 1/8 of 5MHz. The clock speed of MPU drives the UART baud rate.

What is the maximum speed of the two communications ports? What is the limitation on the optical port? What are the available divide ratios for the baud rate generator?

We have run the COM ports at 38.4kbaud and believe they can go faster with more care in the 80515 MPU program. The two COM ports are the same, with the exception that the optical port has an analog comparator on its RX and a tri-statable output driver on its TX. Software setup for both ports is slightly different. The available baud rates are 2400, 4800, 9600,19.2, 38.4, 76.8, 153.6, but the 80515 MPU may not be able to keep up with baud rates above 38.4kbaud. The 115.2kbaud family is not available.

What is the speed of I2C on the DIO04 and DIO05?

The I^2C speed is 78kHz.

What are the choices for a digital interface to the 71M6513/11 devices?

1. SPI master (output only). The RTM output permits 4 selected 32 bit words to be output each CE code pass. The code passes are at 2,520Hz rate, resulting in an average throughput of 322kbps. Each group of 4 words can be output at 5MHz bit rate, with a long pause until the next code pass. During the gap, the 80515 MPU could select a different list of output words. This is the fastest and easiest way to output 16 bytes. For customers who want to output a specific collection of data each frame time, the 80515 MPU could be programmed to sequence the desired words out through the RTM. The control interface could be implemented in I2C, serial port, or be output on general I/O pins using the bit bang scheme.
2. I^2C - Master only. The clock rate is 78kHz. If the external processor wants to receive values for temperature, frequency, Wh, VARh, V^2h, and I^2h, it needs 6*32 = 192 bits each frame. At a 1Hz frame rate, this is easily within the capability of the I^2C interface. Being unable to implement slave mode may be a problem if the processor wants to talk to other I^2C devices.
3. Bit banged parallel. In block mode, this could be as fast as 100kHz word rate (16 bit word). If a handshake is used for each word, the rate probably drops to 10kHz. There is a concern here that the 71M651X couldn't recognize a write strobe fast enough to recognize the data.
4. Serial port. This port can run faster than 9,600 baud. But even at 9,600 baud it is fast enough to transfer 192 bits per frame.

What is RTM?

RTM stands for Real Time Monitor. RTM is programmed through the debug board to monitor Compute Engine RAM data. Please refer data sheet for more RTM timing info. RTM data can be connected to a DSP or other external equipment to obtain and analyze raw sample data.

ICE, Programming, Debugging and Firmware

Is the debug port that appears on the 71M6511 and 71M6513 demo boards a JTAG port?

The debug port is not a JTAG port per IEEE 1149. The debug port is used for connecting a PC COM port (serial port) to the chip via the Debug Board. This will give the user an option for observing and altering internal parameters of the meter device by connecting a terminal or by using PC terminal software.

Does the ADM51 ICE function well when connected to the 71M651x demo boards during 'live' measurements?

Yes. There is no change to the accuracy with the ICE connected or disconnected. The same is true of the Debug Board.

Is the LCD API flexible, i.e. will it support the full range of displays that can be supported by our hardware, or are there some restrictions? I am planning to design our own proprietary display. Would the LCD API be configurable to suit this?

The TDK 71M6511/13 devices can drive the segment and back plane lines of the LCD directly. Within each chip, each addressable segment is independently controlled. Thus, to the extent permitted by the number of segment drivers, the part should be able to interface to any custom LCD. The structure inside the LCD API needs to be modified for the current segment mapping.

Is Keil's C compiler/assembler/linker required for the 71M6151x devices? How about other tools?

We are using Keil's C tools. Other tools can potentially be used, but we have not tested any. The ultimate goal is to generate a hex file that is compatible to upload to the MPU flash memory of the device.

What is the utility we can use to re-flash the 71M651X part after re-compiling the DSP code and firmware code respectively?

We use the Signum ICE (model ADM51) for flash uploading during development. A Flash Download Board will be available for programming of production units.

Tamper Detection

Do the 71M651x devices support tampering detection?

Yes, the 80515 MPU code can be programmed for tampering detection based on the technique and sensor used for detection.

EMI/EMC

Does TDK have any EMI test data for the 71M651x power meter chips?

No EMI testing has been done on the ICs themselves. EMI always has to be tested in a complete system. However, TDK has performed ESD testing and all pins of the wattmeter chips surpass TDK's 2000V ESD specification.

Do the Demo Boards meet conductive and radiated emission testing?

The revisions A of the 71M6511 and 71M6513 Demo boards have been tested for conductive and radiated emissions in compliance with FCC Class B part 15.

Voltage/Power Requirements, Battery Operation

Can the V3P3D/V3P3A devices be powered in battery back-up mode, so that the MPU can respond to a key press and briefly display data on the LCD, or perform some communications via the serial interface?

It is possible to implement this procedure. The current Demo Board does not support it directly. However, the MPU can be programmed to run in low-power mode using one of the DIO pins to sense the power fail. Upon power fail the MPU is powered by battery, and the firmware will shut down the CE, ADC, LCD boost and other circuitry in order to save power. The V3P3D/V3P3A pins must be tied together and GNDA and GNDD must be tied together.

How low can the battery voltage be in the 71M651X devices?

The minimum voltage of operation we suggest is 3.00V even though the 651x has lot of margin below 3V. V1 has to be tied to battery backup to prevent a reset.

Demo Board Questions

What program is pre-installed on the 71M6513 IC with the demo board?

The program pre-installed in the 71M6513/6511 IC that comes with the board is the demo program that is released at the time of shipment (filename 651X_demo.hex). The release date of the program can be determined by typing the command **>i1** (letter i, followed by the digit "one") using the serial interface.

Is the voltage on the demo boards 5V even though the IC runs on 3.3V?

Yes. It is 5V and is regulated down to 3.3V on the demo board.

What are the two rates for the fast/slow switch SW1 that controls the Wh/VAR pulse outputs in the TDK 71M651x devices?

FAST is 0.23 Wh (828Ws) per pulse. This will allow the user to test the meter for low currents.
SLOW is 3.68 Wh (13,248Ws) per pulse. This allows for meter testing at high currents.
However, the current Demo Board code does not read the position of switch SW1. Recent 6511 Demo Boards are shipped with SW1 removed.

What Kh is programmed into the Demo Boards for the TDK 71M651x devices?

The 71M6513/6513H Demo Boards have a Kh of 3.2 (Wh per pulse), if they are operated with an external CT (current transformer) that has a winding ratio of 2,000:1. These values can be derived by reading the values for IMAX and VMAX (i.e. the RMS current and voltage values that correspond to the 250mV maximum input signal to the IC), which should be 208A and 600V, and inserting them in the equation for Kh:

$Kh = IMAX * VMAX * 5.7703*10^{-3} * 16384 / (3600 * WRATE) = 3.2Wh$

WRATE (CE register location 2D) is 1024.

For the 71M6511/6511H, WRATE is 2334 so that the equation becomes:

$Kh = IMAX * VMAX * 4.11021*10^{-3} * 16384 / (3600 * 2334) = 1.0Wh$

How would I conduct EMI testing on the Demo Board?

The Demo Board is not a reference design and it is not optimized for EMI. As a starting point, the Demo Board may be operated in an EMI laboratory in order to test electromagnetic emissions and susceptibility. The layout of the Demo Board is not optimized for EMI emissions. Similarly, the Demo Board does not have provisions for protection against high-energy bursts. Tranzorbs, MOVs, capacitors and the like must be added to properly protect the Demo Board. ESD discharges directly to the Demo Board surface and/or LCD must be avoided. As in a finished meter product, a certain distance (e.g. one inch) between the viewing window and the display has to be maintained for ESD immunity.

How can I test power-down, brown-out and battery operation with the Demo Board?

Power-down, brown-out and battery operation can easily be simulated and evaluated with the Demo Board. A 3.6 volt battery should be connected at the two-pin header labeled “PT1”, and the corresponding jumper at JP8 should be connected between the pins “VBAT” and “BATTERY”. With the 5V power supply removed, the battery current drawn by the 71M6513/6513H or 71M6511/6511H can easily be verified by connecting a DMM between the BT1 header and the battery. Power sags and brown-outs can be simulated by modulating the 5V power supply and verifying that all functions (RTC, XRAM) are properly maintained while the main power is down.

Note: Revisions A and B02 of the 71M6513/6513H or 71M6511/6511H will loose the RTC while power is down, even if a battery is attached.

How can I test power consumption of the chip on the Demo Board?

When power consumption is measured it should be noted that the shunt regulators will cause relatively high consumption when using the supplied 5V power supply. This is due to their function similar to zener diodes, i.e. causing a voltage drop of 5V – 3.3V across a low-ohmic resistor. Once, a regulated power supply is used and adjusted close to 3.3V, the total power consumption of the Demo Board will drop rapidly, giving a good indication of the chip’s potential performance. A few components around the 71M6513/6513H or 71M6511/6511H will contribute to the power consumption as will the operation mode of the chip. See the section “Power Saving Measures” located in the appendix of the Demo Board User’s Manual for a detailed description of how power can be saved.

How can I access the I/O memory using the serial commands that come with the Demo Board?

The following command lets you read and write all I/O memory locations:

>RI20$ reads hex value at address 2020 (LCD_BSTEN)

>RI20=0E writes hex value 0E into address 2020

My CT has only a turn ratio of 1000:1. How can I modify my Demo Board to accommodate this?

The basic scaling conditions for the demo board are:
VMAX = 600V and IMAX = 208A.
208A would generate 104mA with a 1:2,000 turns ratio. These 104mA would generate 176mV RMS across resistors R24, R25 (1.7Ω total), or 250mV peak at the IA input. I you are using a 1:1,000 turns ratio, you would generate 208mA at 208A. This means you should decrease the resistors R24, R25 and so forth so the combined resistance is 0.85Ω.

Scale and Other DC Applications

Can the 71M6513 IC be used for DC applications?

Yes, the inputs are useable for both AC and DC.

What offset and noise figures can be expected for a DC application?

1. The 71M651X chips use single converter technology. This means that all channels have the same offset. However, care must be taken to match input impedance between ground sense and signal sense. The typical input impedance is 70kOhms.
2. A typical offset of 2mV has been observed and this offset is tightly matched between parts.
3. We have not characterized the broadband noise since it is not important for power meter applications
4. TDK has developed a scale application. In this application, rather than processing the differential voltage with an instrumentation amplifier, the DC voltage applied between two input channels is measured and then subtracted. Also, the chip temperature is measured. This application uses a 3-pole Gaussian low-pass filter with the following characteristics:

    -119dB @ 50Hz

    -3dB @ 0.28Hz

    Settling time to 0.1%: 3.0 seconds

    Settling time to 1ppm: 4.3 seconds.

The resulting circuit had 4 stable digits of display.

Miscellaneous

Is there a zero crossing for mains locked RTC and can one of the input pins be used as a comparator to interrupt the MPU on each zero crossing in the 71M651x devices? Will this load the ADC voltage input leading to inaccuracies?

Since the built-in RTC is based on the watch crystal, a mains based RTC will be a second RTC implemented entirely in 80515 MPU code, unless approach 3 is used.
Approach 0. Yes, one of the comparators could be used as a 60/50Hz MPU interrupt. This approach requires that the 80515 MPU performs de-bouncing and that one selected phase is hardwired to the comparator. Accuracy effects are also of concern.
Approach 1: There are direct 71M6513 outputs that can be issued by the CE. Presently, the CE demo code uses them as Wh and VARh pulse outputs. One of them could certainly be converted to a glitch free 60/50Hz output and be configured to interrupt the 80515 MPU. [Note that these two outputs are one of the few functions that don't work in our A01 silicon version. Also, the specification states that when configured as outputs, DIO pins can't interrupt the MPU - this is being changed in the B02 version so they can generate interrupts]. This approach permits the CE to select an active phase and perform de-bounce filtering on it. In fact, the CE demo code already does this in the frequency-determining (FLL) module. The question of how the accuracy might be disturbed due to the extra processing performed each mains cycle in the 80515 MPU is a good one and a sound reason why other approaches should be considered first.
Approach 2: The CE can be programmed to accumulate cycle counts during each XFER interval. The demo code creates XFER intervals at approximately a 1Hz rate (corresponding to an exact number of crystal clocks) and interrupts the 80515 MPU when the interval has expired. The XFER interrupt handler is the primary interrupt handler in the 80515 MPU demo code. It reads the CE accumulators and updates the 80515 MPU Wh and Varh registers. It could also be programmed to update its RTC with the count of main cycles occurring during the interval. The advantages of this approach are twofold: There is no 50/60Hz-processing overhead, and the load on the MPU is reduced.
Approach 3: Two new bits have been added to the B02 version of the 6513. These bits allow the MPU to easily add or subtract 1 second from the hardware RTC. The intent is that they permit the RTC to be calibrated and temperature corrected in a way not affecting the meter accuracy. The best approach for mains-locked RTC is to use the cycle count accumulated in approach 2 to determine when the hardware RTC time needs to be corrected. This way, the hardware RTC can be used to keep track of hours, days, months, years, etc. This also provides a seamless method for bridging power outages.

Is there an interrupt available with the output of the energy pulse? Are there interrupt priorities?

Yes there definitely are interrupt priorities and the 80515 MPU code is entirely interrupt driven. The CE pulse output can be configured as an interrupt.

What is the range of pulse rates available from the Wh and VARh test LEDS?

The pulse generators are implemented entirely within the CE and are therefore easily customizable. Since the CE sample rate is 2,520Hz, the maximum pulse rate is half that or 1,260Hz. The demo generators are 32 bit rollover-enabled integrators whose output is their sign bit. They naturally provide a 50% duty cycle. The pulse width could be modified with further CE code. The pulse rate is entirely programmable within the <1,260Hz upper limit.

In the 71M6513, can the V+I samples be re-aligned for each phase, since they may be 7 degrees apart, or are all the samples aligned for all 3 phases or is each phase sample set (V+I) independently?

Each V I pair is phase-aligned to itself and not to the other two pairs. The uncorrected phase error is actually 2/13th of the 2,520Hz period or 1.1 degrees at 50Hz.

What is the accuracy of the frequency measurement?

The frequency measurement in the Demo code can be considered ideally accurate (within the constraints of crystal accuracy) with zero mean AC noise added. The AC noise is 0.25% pp and is averaged away during Watt and VAR measurements.

When the 71M651x devices store the V+I samples, are they the phase-shifted versions, with the INTERP compensation already applied?

Yes.

Is there any way to improve speed on the voltage and current estimates?

Yes, the XFER rate is 1Hz in the demo setup (PRESAMPS=42, SUMCYCLES=60). The rate is highly programmable, however, since it is the 2,520Hz sample rate divided by the product of PRESAMPS and SUM_CYCLES, where PRESAMPS can be 42, 50, 84, or 100 and SUM_CYCLES can be any value from 1 to 63. The concept is that accumulation should occur in two steps: a fast accumulator that accumulates one or two cycles and provides info to the CREEP discriminator, followed by a slower accumulator which slows the 8051 interrupt rate substantially. CE code can be modified for voltage sag/swell. Perhaps this could be done at the same time as CREEP, or perhaps the XFER rate could be increased. If an entirely different circuit is needed, there is still plenty of code space, data RAM, and code cycles available in the CE.

In the 6515 data sheet a zero-cross function is mentioned. Can this be used for synchronizing the RTC to the 50Hz/60Hz mains period?

The main purpose of the zero cross detection is to announce the presence of voltage for the external microcontroller. It is also used by the measurement module of the compute engine for signal processing routines.